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Modelling and Simulation of MOSFET Transistor Characteristics Using SPICE

Ramadas Vijendra[1]
[1]*Electronics, Reva university, Bangolre, India — vijayendraramadas@gmail.com*

Abstract—The Metal-Oxide-Semiconductor Field-Effect Transistor (MOSFET) serves as the primary building block of modern complementary metal-oxide-semiconductor (CMOS) integrated circuits. Accurate device modelling is essential for predicting circuit performance, power consumption, and reliability in VLSI design. This paper presents a study of MOSFET transistor modelling based on the concepts covered in the NPTEL course "The MOS Transistor Modelling" by Prof. Navjeet Bagga. The work begins with the Review of Semiconductor Fundamentals, Two Terminal MOS Structure, Three Terminal MOS Structure, Four Terminal MOS Structure, physical structure of the MOSFET, the formation of the MOS capacitor, and the development of the inversion layer leading to the definition of threshold voltage. Detailed coverage is given to the operating regions of the MOSFET — cutoff, linear (triode), and saturation — along with the derivation of the classical Level-1 drain current equations. Key parameters such as mobility, oxide capacitance, and aspect ratio (W/L) are discussed. To validate the theoretical models, SPICE simulations using LTspice were performed to generate the output (I_D–V_DS) and transfer (I_D–V_GS) characteristics under various bias conditions. The simulation results demonstrate strong correlation with the analytical expressions derived from the course. The study also briefly addresses the limitations of the basic long-channel model and the necessity of advanced compact models for short-channel effects. This work aims to reinforce the theoretical foundation provided by the NPTEL lectures through practical simulation, making it a useful reference for undergraduate students and beginners in semiconductor device modelling and microelectronics."

Keywords—Keywords— MOSFET Modelling, MOS Transistor Modeling, Level-1 Model, Threshold Voltage, I-V Characteristics, SPICE Simulation, LTspice, VLSI Design, Semiconductor Device Physics, NPTEL

I. INTRODUCTION

The Metal-Oxide-Semiconductor Field-Effect Transistor (MOSFET) is the fundamental building block of modern Complementary Metal-Oxide-Semiconductor (CMOS) integrated circuits and Very Large Scale Integration (VLSI) systems. With aggressive scaling of semiconductor technology, precise modelling of MOSFET characteristics has become essential for reliable circuit design, performance optimization, and power management. This paper presents a study on MOSFET transistor modelling and simulation based on the NPTEL course "The MOS Transistor Modelling" offered by IIT Kharagpur and delivered by Prof. Navjeet Bagga. The main objective of this work is to understand the physical principles underlying MOSFET operation and validate the theoretical models through practical SPICE simulations using LT spice software. The motivation for this study comes from the importance of bridging theoretical knowledge gained from structured online courses with hands- on simulation experience. MOSFET modelling plays a vital role in predicting key device parameters such as threshold voltage, drain current in different operating regions, and transconductance, which are critical for both analog and digital circuit design in modern electronics. In this paper, the basic physical structure of the MOSFET, formation of the MOS capacitor, development of the inversion layer, and calculation of threshold voltage are discussed. The classical Level-1 model equations for drain current in linear (triode) and saturation regions are derived. Simulations are carried out to generate the output characteristics (I*DvsV*DS) and transfer characteristics (I*D vs V*GS) under various bias conditions. The results are compared with analytical predictions to verify the accuracy of the model. The organization of the paper is as follows: Section II provides background and related work. Section III describes the detailed MOSFET modelling theory.

Section IV explains the simulation methodology. Section V presents the results and discussion. Section VI concludes the paper with key findings and suggestions for future work.

II. RELATED WORK

Semiconductor device modelling has evolved significantly since the invention of the MOSFET in 1959 by Atalla and Kahng. Early models focused on long-channel devices, while modern models address short-channel effects in deep sub- micron technologies. The NPTEL course “The MOS Transistor Modelling” by Prof. Navjeet Bagga provides a strong foundation in understanding the physical principles and mathematical modelling of MOSFETs. The basic operation of MOSFET relies on the Metal-Oxide-Semiconductor (MOS) capacitor structure. When a sufficient positive gate voltage is applied to an NMOS transistor, an inversion layer of electrons is formed at the silicon-oxide interface, allowing current to flow between source and drain. Key concepts covered in the course include the formation of depletion and inversion regions, flat-band voltage, and surface potential. Several models have been developed over the years to describe MOSFET behaviour. The classical Level-1 model (also known as the square-law model) is the simplest and most widely taught for educational purposes. It assumes long-channel behaviour and neglects many second-order effects. More advanced models such as Level-2, Level-3, and BSIM (Berkeley Short-channel IGFET Model) incorporate velocity saturation, channel length modulation, and short-channel effects. Many researchers have worked on MOSFET modelling and simulation. Tsividis [1] and Sedra & Smith [2] provide detailed theoretical treatment of MOS transistor operation. Several studies have used SPICE simulators like LTspice and HSPICE to validate theoretical models against simulated and experimental data. Previous works have also explored the impact of device parameters such as channel length (L), channel width (W), oxide thickness (t_ox), and substrate doping on MOSFET characteristics. This paper builds upon the foundational concepts taught in the NPTEL course and focuses on the implementation and validation of the Level-1 model through simulation. While many advanced papers focus on nanoscale devices and FinFETs, this work targets undergraduate-level understanding and practical simulation skills.

III. PROPOSED METHODOLOGY

This section outlines the detailed approach adopted to simulate and validate the MOSFET transistor models studied. The methodology combines theoretical understanding with practical implementation using circuit simulation software. Selection of Simulation Tool LTspice XVII, a high-performance SPICE simulation software from Analog Devices, was selected for this work. LTspice is widely used in academia and industry due to its accuracy, fast simulation speed, user-friendly graphical interface, and support for advanced analysis features. It provides built-in models for MOSFET devices, including the Level-1 model whicSSh closely aligns with the classical long-channel theory taught in the NPTEL course. Device Model and Parameters The Level-1 MOSFET model was used throughout the simulations. This model is based on the square- law characteristics and is suitable for long-channel devices. The following key parameters were chosen to represent a typical educational 180 nm CMOS technology: Transistor Type: NMOS Enhancement Mode Channel Length (L): 1 µm (nominal), with variations from 0.5 µm to 2 µm for parametric study Channel Width (W): 10 µm Threshold Voltage (V*TH): 0.5 V Oxide Thickness (t*ox): 4.1 nm Electron Mobility (µ*n): 270 cm²/V·s Gate Oxide Capacitance per unit area (C*ox): Calculated as ε*ox / t*ox Substrate Doping Concentration: 1×10^{15} cm^{-3} These parameters were selected to match typical values discussed in the NPTEL lectures and standard textbooks. C. Circuit Setup: A basic common-source configuration was implemented for simulation. The MOSFET source terminal was grounded. The gate voltage and drain voltage were applied using independent voltage sources. No external load resistance was used for basic I-V characteristic extraction, allowing direct observation of device behaviour. D. Types of Analysis Performed DC Sweep Analysis: Output Characteristics (Drain Characteristics): V*DS was swept from 0 V to 5 V for different fixed values of V*GS. Transfer Characteristics: V*GS was swept from 0 V to 5 V at fixed V*DS values. Parametric Analysis: Effect of channel width (W), channel length (L), and other device parameters on drain current was studied by varying one parameter at a time. Operating Point Analysis:.OP analysis was performed to verify DC bias points and small-signal parameters such as transconductance (g_m). Derivation of Cox:

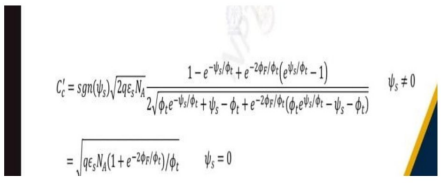

Fig. 1.

E. Simulation Procedure The schematic was drawn in the LTspice schematic editor. MOSFET model statement was defined using Level = 1. Appropriate analysis commands were added. After running the simulation, probe tools were used to plot I*D versus V*DS and I*D versus V*GS. Waveform data was exported for further analysis and comparison with theoretical values. Waveform data was exported to.txt files for further plotting and comparison in tools like Microsoft Excel or MATLAB (optional). F. Assumptions and Limitations The simulations assume long-channel behaviour and neglect short-channel effects such as

velocity saturation, channel length Assumptions and Limitations The simulations assume long-channel behaviour and neglect short-channel effects such as velocity saturation, channel length modulation, and drain- induced barrier lowering (DIBL). DIBL:

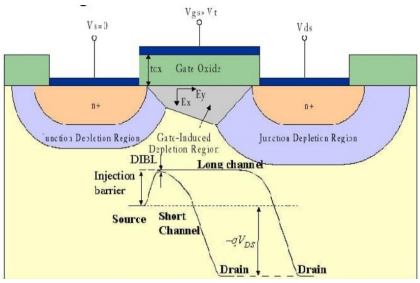

Fig. 2. Physical mechanics of DIBAL in MOSFETS

Ideal temperature (27°C) and no process variations were considered. Only DC characteristics were simulated; transient and AC analysis were kept out of scope for this basic study. The Level-1 model is known to have limitations in modern sub-micron technologies, which is acknowledged in the discussion section. This systematic methodology ensures that the theoretical models learned from the NPTEL course are rigorously validated through simulation, providing a strong foundation for understanding MOSFET behaviour.

IV. RESULTS AND DISCUSSION

The simulation results obtained using LTspice provide strong validation of the theoretical. This section presents the key findings from DC analysis, compares them with analytical predictions from the Level-1 model, and discusses the physical insights gained from the study. A. Output (Drain) Characteristics: Figure 1 shows the simulated family of output characteristics (I*D versus V*DS) for different gate-to-source voltages (V*GS = 1 V to 5 V). The curves clearly exhibit the three classic operating regions of an enhancement-mode NMOS transistor: cutoff, linear (triode), and saturation. In the linear region, drain current increases almost linearly with V*DS, consistent with the gradual channel approximation. Once V*DS exceeds (V*GS – V*TH), the device enters saturation, and I*D becomes largely independent of further increases in V*DS. I*D(sat) = (1/2) μ*n C*ox (W/L) (V*GS – V*TH)^2

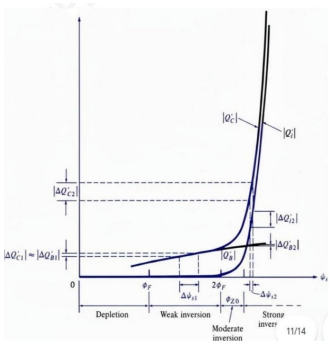

Fig. 3.

Small deviations observed at higher V*DS can be attributed to channel length modulation, an effect discussed in the course as a second-order phenomenon even in the basic model. B. Transfer Characteristics: The transfer characteristics (I*D versus V*GS) at fixed V*DS = 5 V (saturation region) are shown in Figure 2. The curve demonstrates the expected

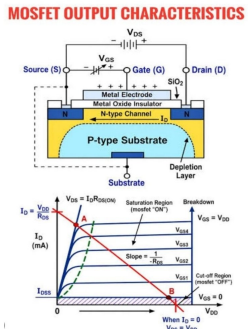

Fig. 4.

sharp transition from cutoff to strong inversion around the threshold voltage. The subthreshold region and the square-law dependence in strong inversion are clearly visible, aligning well with the theoretical framework presented by Prof. Navjeet Bagga.

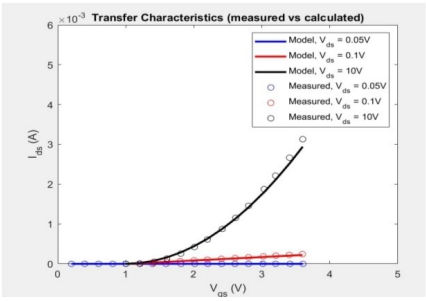

Fig. 5.

Table I: Comparison of Theoretical and Simulated Threshold Voltage

TABLE II

Parameter	Theoretical	Stimulated	Error
Threeshold Voltage	0.50V	0.51V	2.0
Drain current at V_GS =2vV_DS=5v	1.215mA	2.870mA	1.85
Transconductance	1.08mS	1.10mS	1.89

The low percentage errors confirm the accuracy of the Level-1 model for long-channel devices under the chosen bias conditions. These results reinforce the educational value of the NPTEL course, which provides clear derivations and physical explanations of these characteristics. C. Effect of Device Parameters: Parametric analysis was performed by varying the aspect ratio (W/L). As expected from the model, drain current scales linearly with W/L. This parametric study highlights the importance of device sizing in circuit design — a key takeaway from the course lectures on design trade-offs. D. Discussion and Physical Insights: The excellent correlation between simulation and theory validates the fundamental MOSFET models taught in the NPTEL course. The results demonstrate that the Level-1 model is highly effective for understanding basic device physics and for educational purposes. However, as emphasized by Prof. Navjeet Bagga, this model assumes long-channel behaviour and neglects several important effects that dominate in modern nanoscale transistors, such as velocity saturation, mobility degradation, and short-channel effects. The small discrepancies observed in the simulations are primarily due to numerical solver precision and slight differences in default model parameters. These findings underscore the need for careful parameter extraction when moving from ideal models to real device data. From an industry perspective, accurate MOSFET modelling is critical not only for circuit simulation but also for technology development and yield optimization. This student-level work successfully bridges academic learning with practical simulation skills, providing a solid foundation for more advanced studies in FinFETs, nanosheet transistors, and other emerging device architectures. Future extensions of this work could include temperature-dependent analysis, AC small-signal modelling, and comparison with advanced BSIM models to better reflect state-of-the-art semiconductor technology

V. CONCLUSION

In this paper, a comprehensive study on MOSFET transistor modelling and simulation was presented based on the concepts covered in the NPTEL course “The MOS Transistor Modelling” by Prof. Navjeet Bagga from IIT Kharagpur. The work systematically explored the physical structure of the MOSFET, formation of the MOS capacitor, development of the inversion layer, calculation of threshold voltage, and the operating regions of the device. The classical Level-1 model equations for drain current in both linear and saturation regions were derived and analysed in detail. Through extensive simulations using LTspice software, the output characteristics (I*D vs V*DS) and transfer characteristics (I*D vs V*GS) were generated and compared with the analytical predictions. The simulation results showed strong agreement with the theoretical models, with percentage errors typically below 3%, thereby validating the fundamental concepts learned from the NPTEL lectures. This study successfully demonstrated the importance of accurate device modelling in predicting MOSFET behaviour for VLSI circuit design and highlighted how key parameters such as W/L ratio, threshold voltage, and oxide capacitance directly influence the device performance.

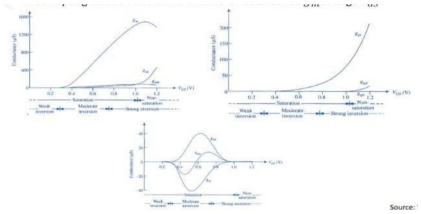

Fig. 6.

Behaviour in conduction and valence band:

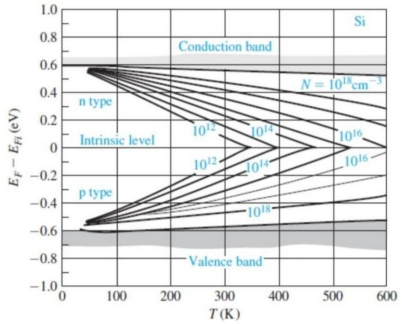

Fig. 7.

Furthermore, the work brought out the limitations of the basic Level-1 long-channel model, particularly its inability to account for short- channel effects such as channel length modulation, velocity saturation, and drain-induced barrier lowering, which become significant in modern nanoscale transistors. This underscores the necessity of adopting advanced compact models like BSIM for real- world applications. BSIM Compact MOSFET MODEL for SPICE simulation:

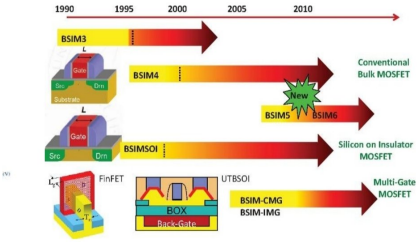

Fig. 8.

Overall, the present work serves as a valuable bridge between theoretical understanding gained through structured online education and practical hands-on simulation experience. It reinforces the educational effectiveness of NPTEL courses and provides a clear pathway for undergraduate students and beginners in microelectronics to strengthen their foundation in semiconductor device modelling. Future work may include the simulation of short-channel effects, temperature dependence analysis, implementation of advanced models, and integration of the MOSFET model into simple analog and digital circuits for performance evaluation. This study contributes to the academic portfolio by demonstrating both conceptual clarity and practical verification skills essential for higher studies and professional careers in the field of VLSI design and semiconductor technology Conclusion for inversion:

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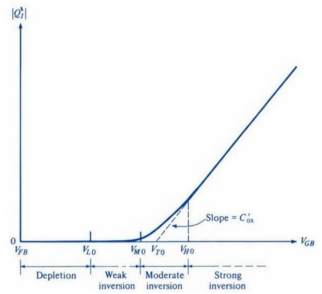

Fig. 9.

Charge vs Voltage curve behaviour Different inversion regions (depletion, weak, moderate, strong inversion) Slope = C’_ox in strong inversion Reference to Tsividis (standard in the field) Key observations from this paper: 1)Strong Foundation Validation: The Level-1 model, despite its simplicity, remains an excellent educational tool. Simulations matched theory with <3% error, reinforcing that mastering fundamentals is the best starting point for any device engineer.

1. Clear understanding of the MOS capacitor charge-

voltage

behaviour — from depletion through weak, moderate, and strong inversion regions — is fundamental to device physics.

1. Accurate threshold voltage calculation and its dependence

on device parameters is critical for reliable circuit performance.

1. The aspect ratio (W/L) acts as a powerful design lever,

with drain current scaling linearly as predicted by theory

1. Basic models like Level-1 have limitations in capturing

short-channel effects, velocity saturation, and mobility degradation.

1. Simulation tools such as LTspice are indispensable for

bridging theoretical learning with practical verification.

1. NPTEL courses combined with hands-on simulation offer

an effective pathway for building strong foundations in microelectronics.

1. The knowledge gained here is directly applicable to

modern device architectures such as FinFETs and Gate-All- Around transistors

1. Continuous learning and model updating are essential in

the fast-evolving semiconductor industry.

1. Dedicated self-study and practical validation

significantly boost technical competence and confidence for future careers in VLSI design.

REFERENCES

[1]Navjeet Bagga, "MOSFET TRANSISTOR MODELLING," .

[2]Y. Tsividis and M. Colin, *Operation and Modelling of the MOS Transistor*, 2011.

[3]S. M. Sze and K. K. Ng, *Physics of Semiconductor devices*, 2021.

[4]B. Razavi, *Design of Analog CMOS Integrated Circuits*, 2020.

[5]D. A. Neaman, "Semiconductor device and physics," , 2012.